DDR2 Fully Buffered Memory Module

AETx61FBxx-[30D/25D]xxxX

512MB, 1GB, 2GB and 4GB

This Data Sheet describes AENEON DDR2 Fully Buffered DIMM on 240-pin modules with parity bit for address and control bus and its main characteristics.

Key features

- Fully buffered DDR2 memory modules
- Available in single pack of densities 512MB/1GB/2GB/4GB
- Standard JEDEC pin configuration
- Validated by major motherboard vendors
- Fully RoHS compliant
- MBIST and IBIST test function
- Uses Advanced Memory Buffer [AMB] to effectively control and manages memory traffic
  - Supports channel initialisation
  - Supports the forwarding of southbound and northbound frames, servicing requests directed to a specific AMB or DIMM, and merging the data in northbound frames
  - Detects errors on the channel and reports them to the host memory controller
  - Supports FB-DIMM configuration register set
  - Acts as DRAM memory buffer for all operations
  - Provides logic to support MEMBIST and IBIST design for test functions
- Module size of 133.35 x 30.35 x 8.2 (mm)
- Fully buffered DIMMs comes with heat sink

TABLE 1
Ordering Information

Product Type[1)]	Module Density	Organization	Rank Organization	Module Speed	No of Comp	Module Size (mm)
DDR2-667, PC2-5300-555						
AET661FB00-30DB19X	512MB	64M x 72	1Rx8	PC2-5300-555	8	133.35 x 30.35 x 8.2
AET761FB00-30DB19X	1GB	128M x 72	2Rx8		18	
AET761FB28-30DB29X	1GB	128M x 72	2Rx4		18	
AET861FB00-30DB19X	2GB	256M x 72	2Rx4		36	
AET861FB28-30DC20X	2GB	256M x 72	2Rx8		18	
AET961FB00-30DC10X	4GB	512M x 72	2Rx4		36	
AET961FB48-30DC20X	4GB	512M x 72	4Rx8		36	
DDR2-800, PC2-6400-555						
AET861FB28-25DC20X	2GB	256M x 72	2Rx8	PC2-6400-555	18	133.35 x 30.35 x 8.2
AET961FB48-25DC20X	4GB	512M x 72	4Rx8		36	

1) Full Product Type / Sales Description

TABLE 2
Speed Grade Definition

Speed Grade		PC2	–6400		–5300			
CAS-RCD-RP latencies			5–5–5		5–5–5			
Parameter		**Symbol**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**	**Note**
Clock Period	@ CL = 3	t_{CK}	5	8	5	8	ns	1)2)3)4)
	@ CL = 4	t_{CK}	3.75	8	3.75	8	ns	1)2)3)4)
	@ CL = 5	t_{CK}	2.5	8	3	8	ns	1)2)3)4)
	@ CL = 6	t_{CK}	2.5	8	—	—	ns	1)2)3)4)
	@ CL = 7	t_{CK}	2.5	8	—	—	ns	1)2)3)4)5)
Row Active Time		t_{RAS}	45	70k	45	70k	ns	1)2)3)4)5)6)
Row Active Time		t_{RAS}	40	70k	40	70k	ns	1)2)3)4)5)7)
Row Cycle Time		t_{RC}	57.5	—	60	—	ns	1)2)3)4)
Row Cycle Time		t_{RC}	52.5	—	55	-	ns	1)2)3)4)
RAS-CAS-Delay		t_{RCD}	12.5	—	15	—	ns	1)2)3)4)
Row Precharge Time		t_{RP}	12.5	—	15	—	ns	1)2)3)4)

1) Timings are guaranteed with CK/$\overline{CK}$ differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode.
2) The CK/$\overline{CK}$ input reference level (for timing reference to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross. The DQS / $\overline{DQS}$, RDQS / $\overline{RDQS}$, input reference level is the crosspoint when in differential strobe mode.
3) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, CKE = 0.2 x V_{DDQ}
4) The output timing reference voltage level is V_{TT}.
5) $t_{RAS.MAX}$ is calculated from the maximum amount of time a DDR2 device can operate without a refresh command which is equal to 9 x t_{REFI}.
6) Products released after 2007-08-01 can support $t_{RAS.MIN}$ = 40 ns for all DDR2 speed sort.
7) For products released after 2007-08-01.

Operating conditions

This chapter describes the operating conditions.

TABLE 3
DC Operating Conditions

Parameter	Symbol	Limit Values			Unit	Notes
		Min.	Nom.	Max.		
AMB Supply Voltage DC	V_{CC}	1.455	1.5	1.575	V	1)
AMB Supply Voltage DC + AC		1.425	1.5	1.590	V	2)
DRAM Supply Voltage	V_{DD}	1.7	1.8	1.9	V	–
Termination Voltage	V_{TT}	0.48 ×V_{DD}	0.50 ×V_{DD}	0.52 ×V_{DD}	V	–
EEPROM Supply Voltage	V_{DDSPD}	3.0	3.3	3.6	V	–
DC Input Logic High(SPD)	$V_{IH(DC)}$	2.1	—	V_{DDSPD}	V	3)
DC Input Logic Low(SPD)	$V_{IL(DC)}$	—	—	0.8	V	3)
DC Input Logic High(RESET)	$V_{IH(DC)}$	1.0	—	—	V	4)
DC Input Logic Low(RESET)	$V_{IL(DC)}$	—	—	+0.5	V	3)
Leakage Current (RESET)	I_L	–90	—	+90	µA	4)
Leakage Current (Link)	I_L	–5	—	+5	µA	5)

1) At 0KHz - 30KHz
2) AT 30KHz - 1 MHz
3) Applies for SMB and SPD Bus Signals
4) Applies for AMB CMOS Signal RESET
5) For all other AMB related DC parameters, contact AENEON technical staff.

TABLE 4
Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Notes
		Min.	Max.		
Voltage on any SMbus interface signal pin relative to V_{SS}	V_{IN}, V_{OUT}	–0.5	+4.00	V	1)
Voltage on V_{DD} pin relative to V_{SS}	V_{DD}	–0.5	+2.4	V	2)
Voltage on V_{CC} pin relative to V_{SS}	V_{CC}	–0,3	+1.75	V	–

Parameter	Symbol	Rating		Unit	Notes
		Min.	Max.		
Voltage on V_{DDQ} pin relative to V_{SS}	V_{DDQ}	–0.5	+2.3	V	2)3)
Voltage on V_{DDL} pin relative to V_{SS}	V_{DDL}	–0.5	+2.3	V	2)3)
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	–0.3	+1.75	V	2)
Voltage on V_{TT} pin relative to V_{SS}	V_{TT}	–0.5	+2.3	V	–
Storage Temperature	T_{STG}	–55	+100	°C	2)3)

1) Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2) When V_{DD} and V_{DDQ} and V_{DDL} are less than 500 mV; V_{REF} may be equal to or less than 300 mV.
3) Storage Temperature is the case surface temperature on the center/top side of the DRAM.

Attention:Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TABLE 5
FB-DIMM Latency Range

Parameter	DDR2–800D			DDR2–667D			Unit	Note
	Min.	Nom.	Max.	Min.	Typ.	Max.		
t_{C2D_DIMM}	Tbd	19.35	Tbd	17.5	21	21.5	ns	1)2)
$t_{RESAMPLE_DIMM_SB}$	Tbd	1.68	Tbd	1.4	1.69	2.4	ns	2)3)
$t_{RESAMPLE_DIMM_NB}$	Tbd	1.48	Tbd	1.3	1.73	2.3	ns	2)4)
$t_{RESYNC_DIMM_SB}$	Tbd	2.66	Tbd	2.5	2.8	3.7	ns	2)5)
$t_{RESYNC_DIMM_NB}$	Tbd	2.54	Tbd	2.4	2.8	3.6	ns	2)6)

1) For DDR-800D and DDR-800E no industry standard values are avalible for Min. and Max parameter.
2) Measured delay at FB-DIMM gold finger between the center of the1st UI of command frame on the primary southbound lane 81 (connector pins 102 & 103) and the center of the 1st UI of return data on the primary northbound lane 0 (connector pins 22 & 23) – [CL (DRAM CAS latency) value] * [frame clock period – AL (DRAM additional latency) value * frame clock period].
3) Measured delay at FB-DIMM gold finger between the center of the 1st UI of a frame on the primary southbound lane 8 (connector pins 102 & 103) and the center of the 1st UI of the same frame on the secondary southbound lane 8 (connector pins 222 & 223).
4) Measured delay at FB-DIMM gold finger between the center of the 1st UI of a frame on the secondary northbound lane 0 (connector pins 142 & 143) and the center of the 1st UI of the same frame on the primary northbound lane 0 (connector pins 22 & 23).

5) Measured delay at FB-DIMM gold finger between the center of the 1st UI of a frame on the secondary northbound lane 0 (connector pins 142 & 143) and the center of the 1st UI of the same frame on the primary northbound lane 0 (connector pins 22 & 23).
6) Measured delay at FB-DIMM gold finger between the center of the1st UI of command frame on the primary southbound lane 81 (connector pins 102 & 103) and the center of the 1st UI of return data on the primary northbound lane 0 (connector pins 22 & 23) – [CL (DRAM CAS latency) value] * [frame clock period – AL (DRAM additional latency) value * frame clock period].

Information

To obtain more information about these products, please contact your AENEON representative.

Please Note
The information herein is given to describe certain components and shall not be considered as a guarantee of characteristics. Terms of delivery and rights to technical change reserved. We hereby disclaim any and all warranties, including but not limited to warranties of non-infringement, regarding circuits, descriptions, and charts stated herein.

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Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest distribution partner.

Components may only be used in life support devices or systems with the express written approval of Qimonda AG, if a failure of such components can reasonably be expected to cause the failure of that life support device or system, or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.